**10UT** 

1IN-

**GND** 

1IN+ [

8 DVDD

7 1 20UT

6 ☐ 2IN-

5 ¶ 2IN+

D, JG, P, OR PW PACKAGE (TOP VIEW)

**FK PACKAGE** 

(TOP VIEW)

2

3

Trimmed Offset Voltage:

TLC277 . . . 500  $\mu$ V Max at 25°C, V<sub>DD</sub> = 5 V

- Input Offset Voltage Drift . . . Typically 0.1 μV/Month, Including the First 30 Days
- Wide Range of Supply Voltages Over Specified Temperature Range:

0°C to 70°C . . . 3 V to 16 V -40°C to 85°C . . . 4 V to 16 V -55°C to 125°C . . . 4 V to 16 V

- Single-Supply Operation
- Common-Mode Input Voltage Range Extends Below the Negative Rail (C-Suffix, I-Suffix types)
- Low Noise . . . Typically 25 nV/√Hz at f = 1 kHz
- Output Voltage Range Includes Negative Rail
- High Input impedance . . . 10<sup>12</sup> Ω Typ
- ESD-Protection Circuitry
- Small-Outline Package Option Also Available in Tape and Reel
- Designed-In Latch-Up Immunity

#### 2 20 19 1 ″<sub>18</sub>∏ NC NC **20UT** 1IN-5 NC NC 16 6 1IN+ 2IN-15 NC П 8 NC 10 11 12 13

NC - No internal connection

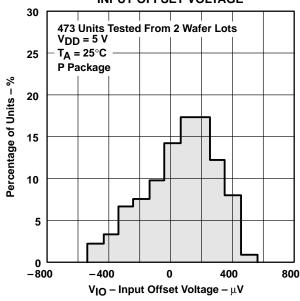
## description

The TLC272 and TLC277 precision dual operational amplifiers combine a wide range of input offset voltage grades with low offset voltage drift, high input impedance, low noise, and speeds approaching those of general-purpose BiFET devices.

These devices use Texas Instruments silicongate LinCMOS $^{\text{TM}}$  technology, which provides offset voltage stability far exceeding the stability available with conventional metal-gate processes.

The extremely high input impedance, low bias currents, and high slew rates make these cost-effective devices ideal for applications previously reserved for BiFET and NFET products. Four offset voltage grades are available (C-suffix and I-suffix types), ranging from the low-cost TLC272 (10 mV) to the high-precision TLC277 (500  $\mu$ V). These advantages, in combination with good common-mode rejection and supply voltage rejection, make these devices a good choice for new state-of-the-art designs as well as for upgrading existing designs.

# DISTRIBUTION OF TLC277 INPUT OFFSET VOLTAGE



LinCMOS is a trademark of Texas Instruments.

SLOS091E - OCTOBER 1987 - REVISED FEBRUARY 2002

## description (continued)

#### **AVAILABLE OPTIONS**

			PAC	KAGED DEVI	CES		OUID
T <sub>A</sub>	V <sub>IO</sub> max AT 25°C	SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	TSSOP (PW)	CHIP FORM (Y)
0°C to 70°c	500 μV 2 mV 5 mV 10mV	TLC277CD TLC272BCD TLC272ACD TLC272CD	1111	1	TLC277CP TLC272BCP TLC272ACP TLC272CP	   TLC272CPW	— — — TLC272Y
−40°C to 85°C	500 μV 2 mV 5 mV 10 mV	TLC277ID TLC272BID TLC272AID TLC272ID	_ _ _ _	_ _ _ _	TLC277IP TLC272BIP TLC272AIP TLC272IP	  -  -  -	- - -

The D package is available taped and reeled. Add R suffix to the device type (e.g., TLC277CDR).

In general, many features associated with bipolar technology are available on LinCMOS™ operational amplifiers without the power penalties of bipolar technology. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are easily designed with the TLC272 and TLC277. The devices also exhibit low voltage single-supply operation, making them ideally suited for remote and inaccessible battery-powered applications. The common-mode input voltage range includes the negative rail.

A wide range of packaging options is available, including small-outline and chip carrier versions for high-density system applications.

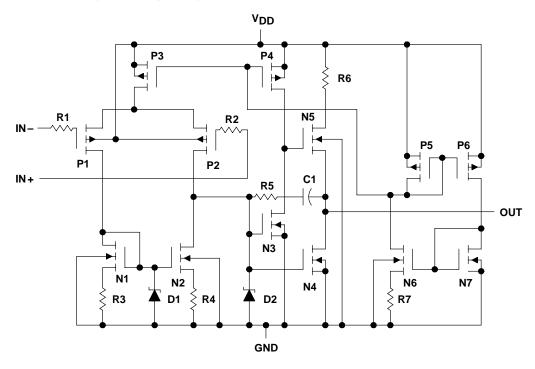
The device inputs and outputs are designed to withstand –100-mA surge currents without sustaining latch-up.

The TLC272 and TLC277 incorporate internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

The C-suffix devices are characterized for operation from  $0^{\circ}$ C to  $70^{\circ}$ C. The I-suffix devices are characterized for operation from  $-40^{\circ}$ C to  $85^{\circ}$ C. The M-suffix devices are characterized for operation over the full military temperature range of  $-55^{\circ}$ C to  $125^{\circ}$ C.

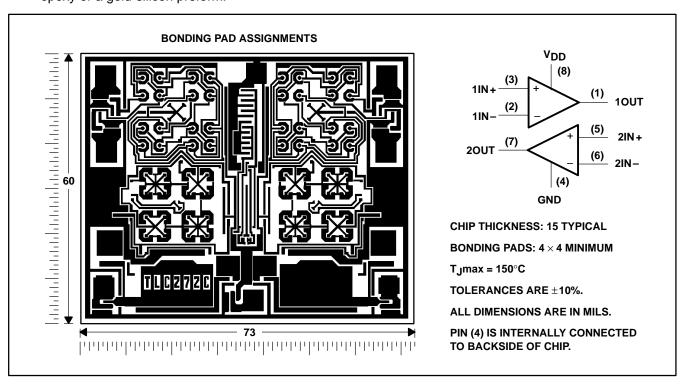


## equivalent schematic (each amplifier)



## **TLC272Y** chip information

This chip, when properly assembled, displays characteristics similar to the TLC272C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.



SLOS091E - OCTOBER 1987 - REVISED FEBRUARY 2002

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V <sub>DD</sub> (see Note 1)	18 V
Differential input voltage, V <sub>ID</sub> (see Note 2)	±V <sub>DD</sub>
Input voltage range, V <sub>I</sub> (any input)	0.3 V to V <sub>DD</sub>
Input current, I <sub>I</sub>	±5 mĀ
output current, IO (each output)	±30 mA
Total current into V <sub>DD</sub>	45 mA
Total current out of GND	
Duration of short-circuit current at (or below) 25°C (see Note 3)	unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature, T <sub>A</sub> : C suffix	0°C to 70°C
l suffix	
M suffix	–55°C to 125°C
Storage temperature range	65°C to 150°C
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, P, or PW p	
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package	300°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
  - 2. Differential voltages are at IN+ with respect to IN-.
  - 3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

#### **DISSIPATION RATING TABLE**

PACKAGE	$T_{\mbox{A}} \le 25^{\circ}\mbox{C}$ POWER RATING	DERATING FACTOR ABOVE T <sub>A</sub> = 25°C	T <sub>A</sub> = 70°C POWER RATING	T <sub>A</sub> = 85°C POWER RATING	T <sub>A</sub> = 125°C POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	N/A
FK	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
Р	1000 mW	8.0 mW/°C	640 mW	520 mW	N/A
PW	525 mW	4.2 mW/°C	336 mW	N/A	N/A

## recommended operating conditions

		C SU	C SUFFIX		I SUFFIX		M SUFFIX	
		MIN	MAX	MIN	MAX	MIN	MAX	UNIT
Supply voltage, V <sub>DD</sub>		3	16	4	16	4	16	V
Occasion and investment V	V <sub>DD</sub> = 5 V	-0.2	3.5	-0.2	3.5	0	3.5	V
Common-mode input voltage, V <sub>IC</sub>	V <sub>DD</sub> = 10 V	-0.2	8.5	-0.2	8.5	0	8.5	V
Operating free-air temperature, TA		0	70	-40	85	-55	125	°C



SLOS091E - OCTOBER 1987 - REVISED FEBRUARY 2002

# electrical characteristics at specified free-air temperature, $V_{DD} = 5 \text{ V}$ (unless otherwise noted)

	PARAMETER		TEST CONDI	TIONS	T <sub>A</sub> †	TLC272 TLC272	C, TLC2 BC, TLC		UNIT
						MIN	TYP	MAX	
		TI 00700	V <sub>O</sub> = 1.4 V,	V <sub>IC</sub> = 0,	25°C		1.1	10	
		TLC272C	$R_S = 50 \Omega$ ,	$R_L = 10 \text{ k}\Omega$	Full range			12	
		TI 007040	V <sub>O</sub> = 1.4 V,	V <sub>IC</sub> = 0,	25°C		0.9	5	mV
<b> </b> ,,		TLC272AC	$R_S = 50 \Omega$ ,	$R_L = 10 \text{ k}\Omega$	Full range			6.5	
V <sub>IO</sub>	Input offset voltage	TI 0070D0	V <sub>O</sub> = 1.4 V,	V <sub>IC</sub> = 0,	25°C		230	2000	
		TLC272BC	$R_S = 50 \Omega$ ,	$R_L = 10 \text{ k}\Omega$	Full range			3000	
		TI 00770	V <sub>O</sub> = 1.4 V,	V <sub>IC</sub> = 0,	25°C		200	500	μV
		TLC277C	$R_S = 50 \Omega$ ,	$R_L = 10 \text{ k}\Omega$	Full range			1500	
$\alpha_{\text{VIO}}$	Temperature coefficient of input	offset voltage			25°C to 70°C		1.8		μV/°C
	lancet offert suggest (see Note 4)				25°C		0.1	60	^
lio	Input offset current (see Note 4)		V 05V	V 05V	70°C		7	300	рA
	level blee summed (see Nets 4)		$V_0 = 2.5 \text{ V},$	$V_{IC} = 2.5 V$	25°C		0.6	60	A
lΒ	Input bias current (see Note 4)				70°C		40	600	рA
						-0.2	-0.3		
					25°C	to 4	to 4.2		V
VICR	Common-mode input voltage rar (see Note 5)	nge				-0.2	4.2		
	(300 14010 3)				Full range	-0.2 to			V
						3.5			
					25°C	3.2	3.8		
Vон	High-level output voltage		$V_{ID} = 100 \text{ mV},$	$R_L = 10 \text{ k}\Omega$	0°C	3	3.8		V
					70°C	3	3.8		
					25°C		0	50	
VOL	Low-level output voltage		$V_{ID} = -100 \text{ mV},$	$I_{OL} = 0$	0°C		0	50	mV
					70°C		0	50	
					25°C	5	23		
A <sub>VD</sub>	Large-signal differential voltage	amplification	$V_0 = 0.25 \text{ V to 2 V},$	$R_L = 10 \text{ k}\Omega$	0°C	4	27		V/mV
					70°C	4	20		
					25°C	65	80		
CMRR	Common-mode rejection ratio		V <sub>IC</sub> = V <sub>ICR</sub> min		0°C	60	84		dB
					70°C	60	85		
				_	25°C	65	95		
ksvr	Supply-voltage rejection ratio (ΔVDD/ΔVIO)		$V_{DD} = 5 \text{ V to } 10 \text{ V},$	V <sub>O</sub> = 1.4 V	0°C	60	94		dB
	(בייטטים וטו				70°C	60	96		
					25°C		1.4	3.2	
IDD	Supply current (two amplifiers)		V <sub>O</sub> = 2.5 V, No load	$V_{IC} = 2.5 V,$	0°C		1.6	3.6	mA
			110 1000		70°C		1.2	2.6	

<sup>†</sup> Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.



SLOS091E - OCTOBER 1987 - REVISED FEBRUARY 2002

# electrical characteristics at specified free-air temperature, V<sub>DD</sub> = 10 V (unless otherwise noted)

	PARAMETER		TEST CONDI	TIONS	T <sub>A</sub> †	TLC272 TLC272			UNIT
						MIN	TYP	MAX	
		TI 00700	$V_0 = 1.4 V$ ,	V <sub>IC</sub> = 0,	25°C		1.1	10	
		TLC272C	$R_S = 50 \Omega$ ,	$R_L = 10 \text{ k}\Omega$	Full range			12	\/
		TI 007040	V <sub>O</sub> = 1.4 V,	V <sub>IC</sub> = 0,	25°C		0.9	5	mV
.,	lanut affaat valtaas	TLC272AC	$R_S = 50 \Omega$ ,	$R_L = 10 \text{ k}\Omega$	Full range			6.5	
V <sub>IO</sub>	Input offset voltage	TI 0070D0	V <sub>O</sub> = 1.4 V,	V <sub>IC</sub> = 0,	25°C		290	2000	
		TLC272BC	$R_S = 50 \Omega$ ,	$R_L = 10 \text{ k}\Omega$	Full range			3000	.,
		TI 00770	$V_{O} = 1.4 \text{ V},$	V <sub>IC</sub> = 0,	25°C		250	800	μV
		TLC277C	$R_S = 50 \Omega$ ,	$R_L = 10 \text{ k}\Omega$	Full range			1900	
CV/IC	Temperature coefficient of input of	offset voltage			25°C to		2		μV/°C
$\alpha_{VIO}$	remperature coemicient of input of	mset voltage			70°C				μν/ Ο
I <sub>IO</sub>	Input offset current (see Note 4)				25°C		0.1	60	pА
טוי	input onset current (see Note 4)		V <sub>O</sub> = 5 V,	V <sub>IC</sub> = 5 V	70°C		7	300	рΑ
lin	Input bias current (see Note 4)		V() = 5 V,	AIC = 2 A	25°C		0.7	60	pА
IB	input bias current (see Note 4)				70°C		50	600	PΑ
					_	-0.2	-0.3		
	On the second of the second of the second of				25°C	to 9	to 9.2		V
VICR	Common-mode input voltage range (see Note 5)	ge				-0.2	3.2		
	(000 11010 0)			Full range to	V				
						8.5			
					25°C	8	8.5		
Voн	High-level output voltage		$V_{ID} = 100 \text{ mV},$	$R_L = 10 \text{ k}\Omega$	0°C	7.8	8.5		V
					70°C	7.8	8.4		
					25°C		0	50	
VOL	Low-level output voltage		$V_{ID} = -100 \text{ mV},$	$I_{OL} = 0$	0°C		0	50	mV
					70°C		0	50	
					25°C	10	36		
AVD	Large-signal differential voltage a	mplification	$V_0 = 1 \text{ V to 6 V},$	$R_L = 10 \text{ k}\Omega$	0°C	7.5	42		V/mV
					70°C	7.5	32		
					25°C	65	85		
CMRR	Common-mode rejection ratio		V <sub>IC</sub> = V <sub>ICR</sub> min		0°C	60	88		dB
	·				70°C	60	88		
					25°C	65	95		
ksvr	Supply-voltage rejection ratio		$V_{DD} = 5 \text{ V to } 10 \text{ V},$	V <sub>O</sub> = 1.4 V	0°C	60	94		dB
	$(\Delta V_{DD}/\Delta V_{IO})$			•	70°C	60	96		
					25°C		1.9	4	
I <sub>DD</sub>	Supply current (two amplifiers)		V <sub>O</sub> = 5 V, No load	$V_{IC} = 5 V$	0°C		2.3	4.4	mA

<sup>†</sup> Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.



SLOS091E - OCTOBER 1987 - REVISED FEBRUARY 2002

# electrical characteristics at specified free-air temperature, $V_{DD}$ = 5 V (unless otherwise noted)

	PARAMETER		TEST COND	ITIONS	T <sub>A</sub> †		2I, TLC2 2BI, TLC		UNIT
						MIN	TYP	MAX	
		TI 00701	V <sub>O</sub> = 1.4 V,	V <sub>IC</sub> = 0,	25°C		1.1	10	
		TLC272I	$R_S = 50 \Omega$ ,	$R_L = 10 \text{ k}\Omega$	Full range			13	>/
		TI 007041	V <sub>O</sub> = 1.4 V,	V <sub>IC</sub> = 0,	25°C		0.9	5	mV
,,	least offertualisms	TLC272AI	$R_S = 50 \Omega$ ,	$R_L = 10 \text{ k}\Omega$	Full range			7	
V <sub>IO</sub>	Input offset voltage	TI 0070DI	V <sub>O</sub> = 1.4 V,	V <sub>IC</sub> = 0,	25°C		230	2000	
		TLC272BI	$R_S = 50 \Omega$ ,	$R_L = 10 \text{ k}\Omega$	Full range			3500	
		TI 00771	V <sub>O</sub> = 1.4 V,	$V_{IC} = 0$ ,	25°C		200	500	μV
		TLC277I	$R_S = 50 \Omega$ ,	$R_L = 10 \text{ k}\Omega$	Full range			2000	
$\alpha_{VIO}$	Temperature coefficient of input	offset voltage			25°C to 85°C		1.8		μV/°C
	Innut affact assument (and Nata 4)				25°C		0.1	60	^
lo	Input offset current (see Note 4)		\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	V 05V	85°C		24	15	рA
	1 11 11 11 N 1 1 N		$V_{O} = 2.5 \text{ V},$	$V_{IC} = 2.5 V$	25°C		0.6	60	
lΒ	Input bias current (see Note 4)				85°C		200	35	рA
						-0.2	-0.3		
					25°C	to	to		V
VICR	Common-mode input voltage rai (see Note 5)	nge				4	4.2		
	(see Note 5)				Full range	-0.2 to			V
					- un rango	3.5			•
					25°C	3.2	3.8		
Voн	High-level output voltage		V <sub>ID</sub> = 100 mV,	R <sub>L</sub> = 10 kΩ	−40°C	3	3.8		V
•				_	85°C	3	3.8		
					25°C		0	50	
VOL	Low-level output voltage		$V_{ID} = -100 \text{ mV},$	$I_{OL} = 0$	-40°C		0	50	mV
-				<b>V</b> -	85°C		0	50	
					25°C	5	23		
AVD	Large-signal differential voltage	amplification	$V_{O} = 1 \text{ V to 6 V},$	R <sub>L</sub> = 10 kΩ	-40°C	3.5	32		V/mV
				_	85°C	3.5	19		
					25°C	65	80		
CMRR	Common-mode rejection ratio		V <sub>IC</sub> = V <sub>ICR</sub> min		-40°C	60	81		dB
					85°C	60	86		
					25°C	65	95		
ksvr	Supply-voltage rejection ratio (ΔV <sub>DD</sub> /ΔV <sub>IO</sub> )		$V_{DD} = 5 \text{ V to } 10 \text{ V},$	V <sub>O</sub> = 1.4 V	-40°C	60	92		dB
	$(\nabla \Lambda \Omega \Omega ) \nabla \Lambda \Omega )$				85°C	60	96		
					25°C		1.4	3.2	
I <sub>DD</sub>	Supply current (two amplifiers)		V <sub>O</sub> = 2.5 V, No load	$V_{IC} = 2.5 V,$	-40°C		1.9	4.4	mA
			INO IOAU		85°C		1.1	2.4	

<sup>†</sup> Full range is –40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.



SLOS091E - OCTOBER 1987 - REVISED FEBRUARY 2002

# electrical characteristics at specified free-air temperature, V<sub>DD</sub> = 10 V (unless otherwise noted)

	PARAMETER		TEST CONDI	TIONS	T <sub>A</sub> †	TLC272	2I, TLC2 2BI, TLC		UNIT
						MIN	TYP	MAX	
		TI 00701	V <sub>O</sub> = 1.4 V,	V <sub>IC</sub> = 0,	25°C		1.1	10	
		TLC272I	$R_S = 50 \Omega$ ,	$R_L = 10 \text{ k}\Omega$	Full range			13	
		TI 007041	V <sub>O</sub> = 1.4 V,	V <sub>IC</sub> = 0,	25°C		0.9	5	mV
l.,	lanut affaat valta aa	TLC272AI	$R_S = 50 \Omega$ ,	$R_L = 10 \text{ k}\Omega$	Full range			7	
V <sub>IO</sub>	Input offset voltage	TI COZODI	V <sub>O</sub> = 1.4 V,	V <sub>IC</sub> = 0,	25°C		290	2000	
		TLC272BI	$R_S = 50 \Omega$ ,	$R_L = 10 \text{ k}\Omega$	Full range			3500	
		TI 00771	V <sub>O</sub> = 1.4 V,	V <sub>IC</sub> = 0,	25°C		250	800	μV
		TLC277I	$R_S = 50 \Omega$ ,	$R_L = 10 \text{ k}\Omega$	Full range			2900	
(V) (I) (C)	Temperature coefficient of input of	offeet voltage			25°C to		2		μV/°C
ανιο	remperature coemcient of input of	Jiiset voitage			85°C				μν/ Ο
I <sub>IO</sub>	Input offset current (see Note 4)				25°C		0.1	60	pА
ilO	input onset current (see Note 4)		V <sub>O</sub> = 5 V,	V <sub>IC</sub> = 5 V	85°C		26	1000	РΛ
lin	Input bias current (see Note 4)		V() = 5 V,	AIC = 2 A	25°C		0.7	60	pА
IB	input bias current (see Note 4)				85°C		220	2000	pΑ
						-0.2	-0.3		
					25°C	to 9	to 9.2		V
VICR	Common-mode input voltage ran (see Note 5)	ge				9.2			
	(see Note 3)				Full range	-0.2 to			V
						8.5			-
					25°C	8	8.5		
∨он	High-level output voltage		V <sub>ID</sub> = 100 mV,	$R_L = 10 \text{ k}\Omega$	-40°C	7.8	8.5		V
				_	85°C	7.8	8.5		
					25°C		0	50	
VOL	Low-level output voltage		$V_{ID} = -100 \text{ mV},$	$I_{OL} = 0$	-40°C		0	50	mV
-				<u>-</u>	85°C		0	50	
					25°C	10	36		
A <sub>VD</sub>	Large-signal differential voltage a	mplification	$V_0 = 1 \text{ V to 6 V},$	$R_L = 10 \text{ k}\Omega$	-40°C	7	46		V/mV
'		•		_	85°C	7	31		
					25°C	65	85		
CMRR	Common-mode rejection ratio		V <sub>IC</sub> = V <sub>ICR</sub> min		-40°C	60	87		dB
	· · · · · · · · · · · · · · · · · · ·				85°C	60	88		
					25°C	65	95		
ksvr	Supply-voltage rejection ratio		$V_{DD} = 5 \text{ V to } 10 \text{ V},$	VO = 1.4 V	-40°C	60	92		dB
""	$(\Delta V_{DD}/\Delta V_{IO})$				85°C	60	96		
					25°C		1.4	4	
I <sub>DD</sub>	Supply current (two amplifiers)		$V_0 = 5 V$ ,	$V_{IC} = 5 V$	-40°C		2.8	5	mA
			No load		85°C		1.5	3.2	
ļ			1			l		ÿ. <u>–</u>	

<sup>†</sup> Full range is -40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.



SLOS091E - OCTOBER 1987 - REVISED FEBRUARY 2002

# electrical characteristics at specified free-air temperature, $V_{\mbox{\scriptsize DD}}$ = 5 V (unless otherwise noted)

	24244555		TEOT 0011D	ITIONIO	- +	TLC27	2M, TLC	277M	
	PARAMETER		TEST COND	IIIONS	T <sub>A</sub> †	MIN	TYP	MAX	UNIT
		TI 007014	V <sub>O</sub> = 1.4 V,	V <sub>IC</sub> = 0,	25°C		1.1	10	.,
,,	lanut affaat valtana	TLC272M	$R_S = 50 \Omega$ ,	$R_L = 10 \text{ k}\Omega$	Full range			12	mV
V <sub>IO</sub>	Input offset voltage	TI 007714	V <sub>O</sub> = 1.4 V,	V <sub>IC</sub> = 0,	25°C		200	500	
		TLC277M	$R_S = 50 \Omega$ ,	$R_L = 10 \text{ k}\Omega$	Full range			3750	μV
αVIO	Temperature coefficient of input cooltage	offset			25°C to 125°C		2.1		μV/°C
	logist offest compant (see Nieto 4)				25°C		0.1	60	pА
liO	Input offset current (see Note 4)		V- 05V	V:- 0.5.V	125°C		1.4	15	nA
1	lament hims summent (see Note 4)		$V_0 = 2.5 \text{ V}$	$V_{IC} = 2.5 V$	25°C		0.6	60	pА
IB	Input bias current (see Note 4)				125°C		9	35	nA
	Common-mode input voltage ran	ae			25°C	0 to 4	-0.3 to 4.2		٧
VICR	(see Note 5)	3-			Full range	0 to 3.5			٧
					25°C	3.2	3.8		
Vон	High-level output voltage		$V_{ID} = 100 \text{ mV},$	$R_L = 10 \text{ k}\Omega$	−55°C	3	3.8		V
					125°C	3	3.8		
					25°C		0	50	
VOL	Low-level output voltage		$V_{ID} = -100 \text{ mV},$	$I_{OL} = 0$	−55°C		0	50	mV
					125°C		0	50	
					25°C	5	23		
$A_{VD}$	Large-signal differential voltage a	mplification	$V_0 = 0.25 \text{ V to 2 V}$	$R_L = 10 \text{ k}\Omega$	−55°C	3.5	35		V/mV
					125°C	3.5	16		
					25°C	65	80		
CMRR	Common-mode rejection ratio		V <sub>IC</sub> = V <sub>ICR</sub> min		−55°C	60	81		dB
					125°C	60	84		
	Supply-voltage rejection ratio				25°C	65	95		
ksvr	(ΔV <sub>DD</sub> /ΔV <sub>IO</sub> )		$V_{DD} = 5 \text{ V to } 10 \text{ V},$	$V_0 = 1.4 \text{ V}$	−55°C	60	90		dB
	. 55 10/				125°C	60	97		
			V <sub>O</sub> = 2.5 V,	V <sub>IC</sub> = 2.5 V,	25°C		1.4	3.2	
$I_{DD}$	Supply current (two amplifiers)		VO = 2.5 V, No load	VIC = 2.5 V	−55°C		2	5	mA
					125°C		1	2.2	

<sup>†</sup> Full range is –55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.



SLOS091E - OCTOBER 1987 - REVISED FEBRUARY 2002

# electrical characteristics at specified free-air temperature, $V_{DD}$ = 10 V (unless otherwise noted)

PARAMETER			TEST COND	ITIONS	T <sub>A</sub> †	TLC272	M, TLC	277M	UNIT
	PARAWETER		TEST COND	ITIONS	'A'	MIN	TYP	MAX	UNII
		TI COZOM	$V_0 = 1.4 V$ ,	$V_{IC} = 0$ ,	25°C		1.1	10	m\/
\/	lanut offeet volteere	TLC272M	$R_S = 50 \Omega$ ,	$R_L = 10 \text{ k}\Omega$	Full range			12	mV
V <sub>IO</sub>	Input offset voltage	TLC277M	$V_0 = 1.4 V$ ,	$V_{IC} = 0$ ,	25°C		250	800	/
		TLC2//W	$R_S = 50 \Omega$ ,	$R_L = 10 \text{ k}\Omega$	Full range			4300	μV
ανιο	Temperature coefficient of input voltage	offset			25°C to 125°C		2.2		μV/°C
	lamed offers assumed (ass. Nats. 4)				25°C		0.1	60	pА
lio	Input offset current (see Note 4)		., .,	.,,	125°C		1.8	15	nA
			$V_{O} = 5 V,$	AIC = 2 A	25°C		0.7	60	pА
IΒ	Input bias current (see Note 4)				125°C		10	35	nA
V	Common-mode input voltage ra	nge			25°C	0 to 9	-0.3 to 9.2		V
VICR	(see Note 5)				Full range	0 to 8.5			٧
					25°C	8	8.5		
∨он	High-level output voltage		$V_{ID} = 100 \text{ mV},$	$R_L = 10 \text{ k}\Omega$	−55°C	7.8	8.5		V
					125°C	7.8	8.4		
					25°C		0	50	
VOL	Low-level output voltage		$V_{ID} = -100 \text{ mV},$	$I_{OL} = 0$	−55°C		0	50	mV
					125°C		0	50	
	1				25°C	10	36		
AVD	Large-signal differential voltage amplification		$V_0 = 1 \text{ V to 6 V},$	$R_L = 10 \text{ k}\Omega$	−55°C	7	50		V/mV
	a <b>p</b>				125°C	7	27		
					25°C	65	85		
CMRR	Common-mode rejection ratio		V <sub>IC</sub> = V <sub>ICR</sub> min		−55°C	60	87		dB
					125°C	60	86		
	0 1				25°C	65	95		
k <sub>SVR</sub>	Supply-voltage rejection ratio (ΔVDD/ΔVIO)		$V_{DD} = 5 \text{ V to } 10 \text{ V},$	V <sub>O</sub> = 1.4 V	−55°C	60	90		dB
	(= · UU/ = · IU/				125°C	60	97		
					25°C		1.9	4	
$I_{DD}$	Supply current (two amplifiers)		V <sub>O</sub> = 5 V, No load	$V_{IC} = 5 V$ ,	−55°C		3	6	mA
					125°C		1.3	2.8	

<sup>†</sup>Full range is –55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

SLOS091E - OCTOBER 1987 - REVISED FEBRUARY 2002

# electrical characteristics, $V_{DD}$ = 5 V, $T_A$ = 25°C (unless otherwise noted)

	DADAMETED	TEST COM	DITIONS	Т	LC272Y		UNIT
	PARAMETER	TEST CONI	DITIONS	MIN	TYP	MAX	UNII
V <sub>IO</sub>	Input offset voltage	$V_{O} = 1.4 \text{ V},$ R <sub>S</sub> = 50 $\Omega$ ,	V <sub>IC</sub> = 0, R <sub>L</sub> = 10 kΩ		1.1	10	mV
$\alpha_{\text{VIO}}$	Temperature coefficient of input offset voltage				1.8		μV/°C
IIO	Input offset current (see Note 4)	V 0.5.V	V 0.5.V		0.1		pA
I <sub>IB</sub>	Input bias current (see Note 4)	$V_0 = 2.5 \text{ V},$	$V_{IC} = 2.5 V$		0.6		pA
VICR	Common-mode input voltage range (see Note 5)			-0.2 to 4	-0.3 to 4.2		٧
Vон	High-level output voltage	$V_{ID} = 100 \text{ mV},$	R <sub>L</sub> = 10 kΩ	3.2	3.8		V
VOL	Low-level output voltage	$V_{ID} = -100 \text{ mV},$	I <sub>OL</sub> = 0		0	50	mV
AVD	Large-signal differential voltage amplification	V <sub>O</sub> = 0.25 V to 2 V	R <sub>L</sub> = 10 kΩ	5	23		V/mV
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}min$		65	80		dB
ksvr	Supply-voltage rejection ratio (ΔV <sub>DD</sub> /ΔV <sub>IO</sub> )	$V_{DD} = 5 \text{ V to } 10 \text{ V},$	V <sub>O</sub> = 1.4 V	65	95		dB
I <sub>DD</sub>	Supply current (two amplifiers)	V <sub>O</sub> = 2.5 V, No load	V <sub>IC</sub> = 2.5 V,		1.4	3.2	mA

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.

# electrical characteristics, $V_{DD}$ = 10 V, $T_A$ = 25°C (unless otherwise noted)

	DADAMETED	TEST COM	DITIONS	Т	LC272Y		UNIT
	PARAMETER	TEST CONI	DITIONS	MIN	TYP	MAX	UNII
V <sub>IO</sub>	Input offset voltage	$V_{O} = 1.4 \text{ V},$ $R_{S} = 50 \Omega,$	$V_{IC} = 0$ , $R_L = 10 \text{ k}\Omega$		1.1	10	mV
$\alpha_{\text{VIO}}$	Temperature coefficient of input offset voltage				1.8		μV/°C
lο	Input offset current (see Note 4)	V 5V			0.1		pА
I <sub>IB</sub>	Input bias current (see Note 4)	$V_O = 5 V$	$V_{IC} = 5 V$		0.7		pА
VICR	Common-mode input voltage range (see Note 5)			-0.2 to 9	-0.3 to 9.2		V
Vон	High-level output voltage	$V_{ID} = 100 \text{ mV},$	R <sub>L</sub> = 10 kΩ	8	8.5		V
VOL	Low-level output voltage	$V_{ID} = -100 \text{ mV},$	I <sub>OL</sub> = 0		0	50	mV
AVD	Large-signal differential voltage amplification	$V_0 = 1 \text{ V to 6 V},$	R <sub>L</sub> = 10 kΩ	10	36		V/mV
CMRR	Common-mode rejection ratio	V <sub>IC</sub> = V <sub>ICR</sub> min		65	85		dB
ksvr	Supply-voltage rejection ratio (ΔV <sub>DD</sub> /ΔV <sub>IO</sub> )	$V_{DD} = 5 \text{ V to } 10 \text{ V},$	V <sub>O</sub> = 1.4 V	65	95		dB
I <sub>DD</sub>	Supply current (two amplifiers)	V <sub>O</sub> = 5 V, No load	V <sub>IC</sub> = 5 V,		1.9	4	mA

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.



SLOS091E - OCTOBER 1987 - REVISED FEBRUARY 2002

# operating characteristics at specified free-air temperature, $V_{DD} = 5 V$

	Equivalent input noise voltage  Maximum output-swing bandwidth	TEST CO	NDITIONS	TA	TLC272C, TLC272AC, TLC272BC, TLC277C			UNIT
				,,	MIN	TYP	MAX	
				25°C		3.6		
			V <sub>IPP</sub> = 1 V	0°C		4		
CD.	Clausesta at units main	$R_L = 10 \text{ k}\Omega$		70°C		3		Mar
SR	Siew rate at unity gain	C <sub>L</sub> = 20 pF, See Figure 1		25°C		2.9		V/μs
		gara .	V <sub>IPP</sub> = 2.5 V	0°C		3.1		
				70°C		2.5		
٧n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	$R_S = 20 \Omega$ ,	25°C		25		nV/√ <del>Hz</del>
				25°C		320		
Вом	Maximum output-swing bandwidth	$V_O = V_{OH}$ , $R_L = 10 \text{ k}\Omega$ ,	C <sub>L</sub> = 20 pF, See Figure 1	0°C		340		kHz
				70°C		260		
				25°C		1.7		
B <sub>1</sub>	Unity-gain bandwidth	V <sub>I</sub> = 10 mV, See Figure 3	$C_L = 20 pF$ ,	0°C		2		MHz
		See rigure 3		70°C		1.3		
				25°C		46°		
φm	Phase margin	$V_{I} = 10 \text{ mV},$	f = B <sub>1</sub> , See Figure 3	0°C		47°		
	•	ος – 20 με,	oce rigule 3	70°C		43°		

# operating characteristics at specified free-air temperature, $V_{DD}$ = 10 V

	PARAMETER	TEST CO	NDITIONS	TA	TLC272			UNIT			
					MIN	TYP	MAX				
				25°C		5.3					
		$R_L = 10 \text{ k}\Omega$ , $C_L = 20 \text{ pF}$ , See Figure 1	V <sub>IPP</sub> = 1 V	0°C		5.9					
	Olever made and condition made			70°C		4.3		\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \			
SR	Slew rate at unity gain			25°C		4.6		V/μs			
		gara r	V <sub>IPP</sub> = 5.5 V	0°C		5.1		nV/√ <del>Hz</del>			
				70°C		3.8					
Vn	Equivalent input noise voltage	f = 1 kHz, See Figure 2	$R_S = 20 \Omega$ ,	25°C		25		nV/√ <del>Hz</del>			
				25°C		200					
ВОМ	Maximum output-swing bandwidth	$V_O = V_{OH}$ , $R_L = 10 \text{ k}\Omega$ ,					0°C		220		kHz
			See rigure r	70°C		140		]			
				25°C		2.2					
В <sub>1</sub>	Unity-gain bandwidth	V <sub>I</sub> = 10 mV, See Figure 3	$C_L = 20 pF$ ,	0°C		2.5		MHz			
		See Figure 3		70°C		1.8					
				25°C		49°					
φm	Phase margin	$V_{I} = 10 \text{ mV},$ $C_{L} = 20 \text{ pF},$	f = B <sub>1</sub> , See Figure 3	0°C		50°					
	Ç	OL − 20 pi²,	oce i iguie 3	70°C		46°					

SLOS091E - OCTOBER 1987 - REVISED FEBRUARY 2002

# operating characteristics at specified free-air temperature, $V_{DD}$ = 5 V

	PARAMETER	TEST CO	TEST CONDITIONS			TLC272I, TLC272AI, TLC272BI, TLC277I		
				TA	MIN	TYP	MAX	
				25°C		3.6		
			V <sub>IPP</sub> = 1 V	−40°C		4.5		
0.0	Observation of continuous to	$R_L = 10 \text{ k}\Omega$ , $C_L = 20 \text{ pF}$ , See Figure 1		85°C		2.8		\// -
SR	Slew rate at unity gain			25°C		2.9		V/μs
		3.5						
				85°C				
Vn	Equivalent input noise voltage	f = 1 kHz, See Figure 2	$R_S = 20 \Omega$ ,	25°C		25		nV/√ <del>Hz</del>
				25°C		320		nV/√Hz kHz
ВОМ	Maximum output-swing bandwidth	$V_O = V_{OH}$ , $R_L = 10 \text{ k}\Omega$ ,	C <sub>L</sub> = 20 pF, See Figure 1	−40°C		380		
				85°C		250		
				25°C		1.7		
В1	Unity-gain bandwidth	V <sub>I</sub> = 10 mV, See Figure 3	$C_L = 20 \text{ pF},$	−40°C		2.6		MHz
		See rigule 3		85°C		1.2		
				25°C		46°		
φm	Phase margin	$V_{I} = 10 \text{ mV},$ $C_{L} = 20 \text{ pF},$	t = B <sub>1</sub> , See Figure 3	−40°C		49°		
	j	OL = 20 pr ,	occ rigule 3	85°C		43°		

# operating characteristics at specified free-air temperature, $V_{DD}$ = 10 V

	PARAMETER	TEST CO	NDITIONS	TA	TLC272I, TLC272AI, TLC272BI, TLC277I			UNIT
				,,	MIN	TYP	MAX	
				25°C		5.3		
			V <sub>IPP</sub> = 1 V	−40°C		6.8		
0.0	Classical and section and	$R_L = 10 \text{ k}\Omega$ , $C_L = 20 \text{ pF}$ , See Figure 1		85°C		4		\// -
SR	Slew rate at unity gain		V <sub>IPP</sub> = 5.5 V	25°C		4.6		V/μs
				−40°C		5.8		
				85°C		3.5		
Vn	Equivalent input noise voltage	f = 1 kHz, See Figure 2	$R_S = 20 \Omega$ ,	25°C		25		nV/√Hz
			C <sub>L</sub> = 20 pF, See Figure 1	25°C		200		
Вом	Maximum output-swing bandwidth			−40°C		260		kHz
				85°C		130		
				25°C		2.2		
В1	Unity-gain bandwidth	V <sub>I</sub> = 10 mV, See Figure 3	$C_L = 20 pF$ ,	−40°C		3.1		MHz
		See Figure 3		85°C		1.7		
				25°C		49°		
φm	Phase margin	$V_{l} = 10 \text{ mV},$ $C_{L} = 20 \text{ pF},$	f = B <sub>1</sub> , See Figure 3	−40°C		52°		
		OL = 20 pr,	See Figure 3	85°C		46°		

SLOS091E – OCTOBER 1987 – REVISED FEBRUARY 2002

# operating characteristics at specified free-air temperature, $V_{DD} = 5 \text{ V}$

	DADAMETED	TEST CO	NDITIONS	т.	TLC272	2M, TLC	277M	
	PARAMETER	I IESI COI	NDITIONS	TA	MIN	TYP	MAX	UNIT
				25°C		3.6		
			V <sub>IPP</sub> = 1 V	−55°C		4.7		
l <sub>CD</sub>	Class mate at smits main	$R_L = 10 \text{ k}\Omega$		125°C		2.3		\//
SR	Slew rate at unity gain	C <sub>L</sub> = 20 pF, See Figure 1		25°C		2.9		V/μs
		gui e i	V <sub>IPP</sub> = 2.5 V	−55°C		3.7		nV/√ <del>Hz</del>
				125°C		2		
Vn	Equivalent input noise voltage	f = 1 kHz, See Figure 2	$R_S = 20 \Omega$ ,	25°C		25		nV/√ <del>Hz</del>
				25°C		320		
Вом	Maximum output-swing bandwidth	$V_O = V_{OH}$ , $R_L = 10 \text{ k}\Omega$ ,	C <sub>L</sub> = 20 pF,	−55°C		400		kHz
		KL = 10 KS2,	occ rigure r	125°C		230		]
		., ., .,		25°C		1.7		
B <sub>1</sub>	Unity-gain bandwidth	V <sub>I</sub> = 10 mV, See Figure 3	$C_L = 20 \text{ pF},$	−55°C		2.9		MHz
		See Figure 3		125°C		1.1		
		.,,		25°C		46°		
φm	Phase margin	$V_{ } = 10 \text{ mV},$	f = B <sub>1</sub> , See Figure 3	−55°C		49°		
	-	OL = 20 pr ,	ccc i igure o	125°C		41°		

# operating characteristics at specified free-air temperature, $V_{DD}$ = 10 V

	DADAMETED	TEST CO	NDITIONS	-	TLC272	M, TLC	277M	
	PARAMETER	TEST CO	NDITIONS	TA	MIN	TYP	MAX	UNIT
				25°C		5.3		
			V <sub>IPP</sub> = 1 V	−55°C		7.1		
CD.	Class rate at smits main	$R_L = 10 \text{ k}\Omega$ , $C_L = 20 \text{ pF}$ , See Figure 1		125°C		3.1		Miss
SR	Slew rate at unity gain $ \begin{array}{c c} C_L = 20 \text{ pF,} \\ \text{See Figure 1} \end{array} $ $ \begin{array}{c c} 25^{\circ}C \\ \text{V}_{IPP} = 5.5 \text{ V} \end{array} $			25°C		4.6		V/μs
		6.1						
				125°C		2.7		
٧n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	$R_S = 20 \Omega$ ,	25°C		25		nV/√ <del>Hz</del>
	Maximum output-swing bandwidth	$V_O = V_{OH}$ , $R_L = 10 \text{ k}\Omega$ ,	C <sub>L</sub> = 20 pF, See Figure 1	25°C		200		
ВОМ				−55°C		280		kHz
				125°C		110		
				25°C		2.2		
В1	Unity-gain bandwidth	V <sub>I</sub> = 10 mV, See Figure 3	$C_L = 20 pF$ ,	−55°C		3.4		MHz
		Gee rigure 3		125°C		1.6		
				25°C		49°		_
φm	Phase margin	$V_{I} = 10 \text{ mV},$ $C_{L} = 20 \text{ pF},$	f = B <sub>1</sub> , See Figure 3	−55°C		52°		
		ο <sub>L</sub> = 20 μι,	occ rigure 3	125°C		44°		

SLOS091E - OCTOBER 1987 - REVISED FEBRUARY 2002

# operating characteristics, $V_{DD} = 5 \text{ V}$ , $T_A = 25^{\circ}\text{C}$

	PARAMETER		EST CONDITIO	Ne	TLC272Y			LINIT
	PARAMETER	11	EST CONDITIO	NS	MIN	TYP	MAX	UNIT
0.0	Slew rate at unity gain	$R_L = 10 \text{ k}\Omega$ ,	C <sub>L</sub> = 20 pF,	V <sub>IPP</sub> = 1 V		3.6		\// -
SR		See Figure 1		V <sub>IPP</sub> = 2.5 V		2.9		V/μs
Vn	Equivalent input noise voltage	f = 1 kHz,	$R_S = 20 \Omega$ ,	See Figure 2		25		nV/√ <del>Hz</del>
ВОМ	Maximum output-swing bandwidth	V <sub>O</sub> = V <sub>OH</sub> , See Figure 1	$C_L = 20 pF,$	$R_L = 10 \text{ k}\Omega$ ,		320		kHz
B <sub>1</sub>	Unity-gain bandwidth	$V_I = 10 \text{ mV},$	$C_L = 20 pF$ ,	See Figure 3		1.7		MHz
φm	Phase margin	V <sub>I</sub> = 10 mV, See Figure 3	f = B <sub>1</sub> ,	$C_L = 20 pF,$		46°		

# operating characteristics, $V_{DD}$ = 10 V, $T_A$ = 25°C

	PARAMETER	_	EST CONDITIO	NC	Т	LC272Y		UNIT  V/μs  nV/√Hz  kHz
	FARAMETER	•	EST CONDITIO	No	MIN	TYP	MAX	UNIT
CD	Class note at socia	$R_L = 10 \text{ k}\Omega$ ,	$C_L = 20 pF$ ,	V <sub>IPP</sub> = 1 V		5.3		Miss
SR	Slew rate at unity gain	See Figure 1		V <sub>IPP</sub> = 5.5 V		4.6		V/μS
Vn	Equivalent input noise voltage	f = 1 kHz,	$R_S = 20 \Omega$ ,	See Figure 2		25		nV/√ <del>Hz</del>
B <sub>OM</sub>	Maximum output-swing bandwidth	V <sub>O</sub> = V <sub>OH</sub> , See Figure 1	$C_L = 20 pF,$	$R_L = 10 \text{ k}\Omega$ ,		200		kHz
B <sub>1</sub>	Unity-gain bandwidth	V <sub>I</sub> = 10 mV,	C <sub>L</sub> = 20 pF,	See Figure 3		2.2		MHz
φm	Phase margin	V <sub>I</sub> = 10 mV, See Figure 3	f = B <sub>1</sub> ,	C <sub>L</sub> = 20 pF,		49°		

#### PARAMETER MEASUREMENT INFORMATION

## single-supply versus split-supply test circuits

Because the TLC272 and TLC277 are optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit gives the same result.

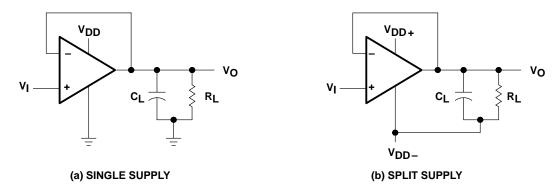


Figure 1. Unity-Gain Amplifier

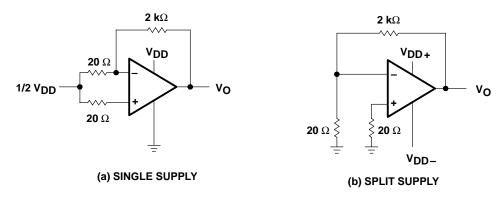


Figure 2. Noise-Test Circuit

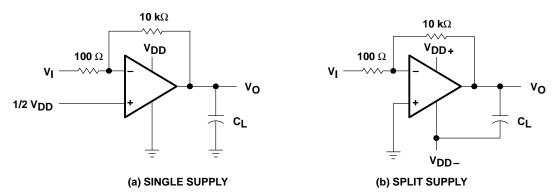


Figure 3. Gain-of-100 Inverting Amplifier



SLOS091E - OCTOBER 1987 - REVISED FEBRUARY 2002

#### PARAMETER MEASUREMENT INFORMATION

## input bias current

Because of the high input impedance of the TLC272 and TLC277 operational amplifiers, attempts to measure the input bias current can result in erroneous readings. The bias current at normal room ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

- 1. Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 4). Leakages that would otherwise flow to the inputs are shunted away.
- 2. Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the open-socket leakage readings from the readings obtained with a device in the test socket.

One word of caution: many automatic testers as well as some bench-top operational amplifier testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into the test socket to obtain a correct reading; therefore, an open-socket reading is not feasible using this method.

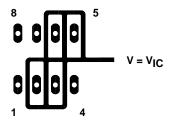


Figure 4. Isolation Metal Around Device Inputs (JG and P packages)

### low-level output voltage

To obtain low-supply-voltage operation, some compromise was necessary in the input stage. This compromise results in the device low-level output being dependent on the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to Figures 14 through 19 in the Typical Characteristics of this data sheet.

### input offset voltage temperature coefficient

Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture results in leakage and contact resistance, which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no effect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. It is suggested that these measurements be performed at temperatures above freezing to minimize error.

SLOS091E - OCTOBER 1987 - REVISED FEBRUARY 2002

#### PARAMETER MEASUREMENT INFORMATION

## full-power response

Full-power response, the frequency above which the operational amplifier slew rate limits the output voltage swing, is often specified two ways: full-linear response and full-peak response. The full-linear response is generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for significant distortion, the full-peak response is specified in this data sheet and is measured using the circuit of Figure 1. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 5). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.

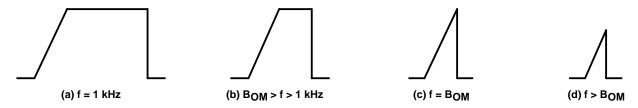


Figure 5. Full-Power-Response Output Signal

#### test time

Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.



SLOS091E - OCTOBER 1987 - REVISED FEBRUARY 2002

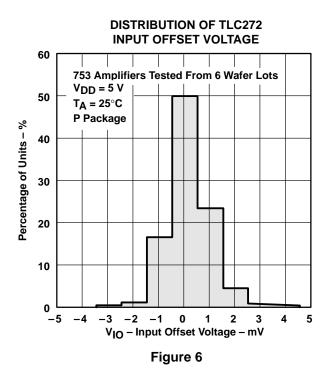
## **TYPICAL CHARACTERISTICS**

## **Table of Graphs**

			FIGURE
VIO	Input offset voltage	Distribution	6, 7
ανιο	Temperature coefficient of input offset voltage	Distribution	8, 9
VOH	High-level output voltage	vs High-level output current vs Supply voltage vs Free-air temperature	10, 11 12 13
V <sub>OL</sub>	Low-level output voltage	vs Common-mode input voltage vs Differential input voltage vs Free-air temperature vs Low-level output current	14, 15 16 17 18, 19
A <sub>VD</sub>	Large-signal differential voltage amplification	vs Supply voltage vs Free-air temperature vs Frequency	20 21 32, 33
$I_{IB}$	Input bias current	vs Free-air temperature	22
lιο	Input offset current	vs Free-air temperature	22
VIC	Common-mode input voltage	vs Supply voltage	23
I <sub>DD</sub>	Supply current	vs Supply voltage vs Free-air temperature	24 25
SR	Slew rate	vs Supply voltage vs Free-air temperature	26 27
	Normalized slew rate	vs Free-air temperature	28
VO(PP)	Maximum peak-to-peak output voltage	vs Frequency	29
B <sub>1</sub>	Unity-gain bandwidth	vs Free-air temperature vs Supply voltage	30 31
φm	Phase margin	vs Supply voltage vs Free-air temperature vs Load capacitance	34 35 36
Vn	Equivalent input noise voltage	vs Frequency	37
	Phase shift	vs Frequency	32, 33



#### TYPICAL CHARACTERISTICS





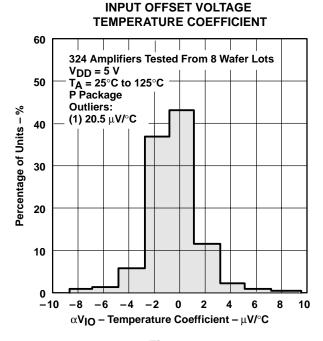


Figure 8

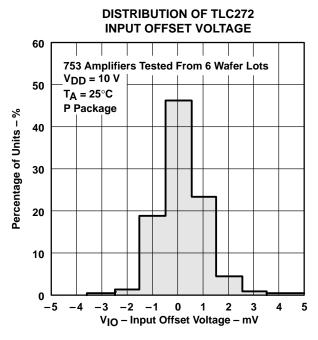


Figure 7

### DISTRIBUTION OF TLC272 AND TLC277 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

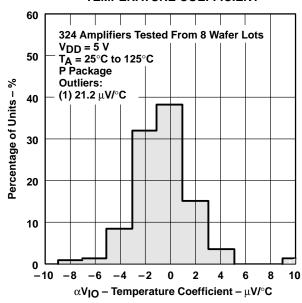
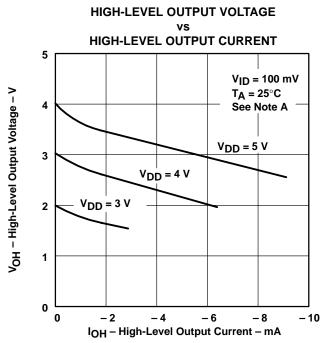


Figure 9



NOTE A: The 3-V curve only applies to the C version.

Figure 10

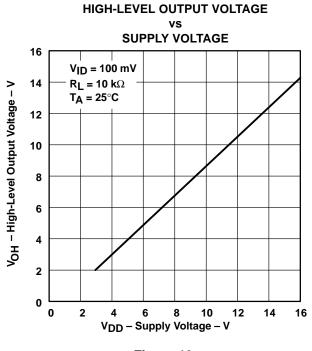


Figure 12

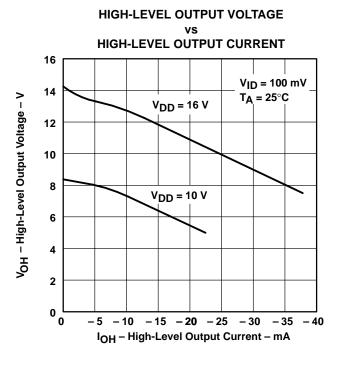
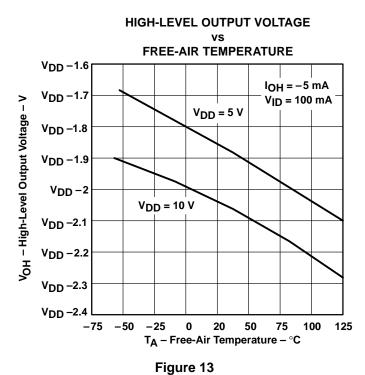
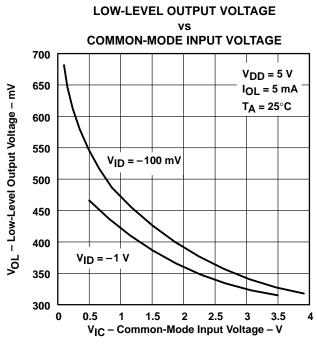


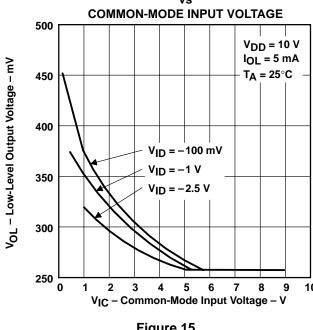
Figure 11



† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.







**LOW-LEVEL OUTPUT VOLTAGE** 

Figure 15

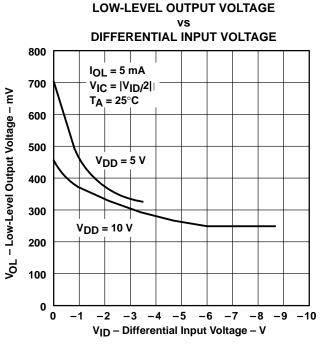
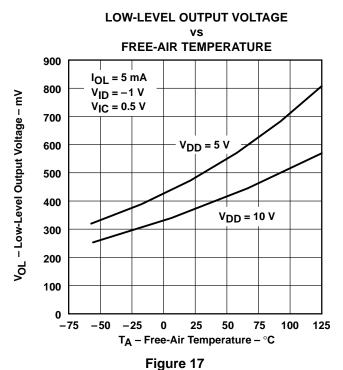
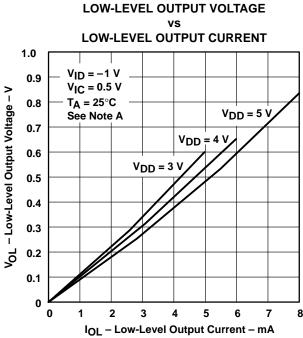


Figure 16



† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.





NOTE A: The 3-V curve only applies to the C version. **Figure 18** 

**LARGE-SIGNAL** 

**DIFFERENTIAL VOLTAGE AMPLIFICATION** 

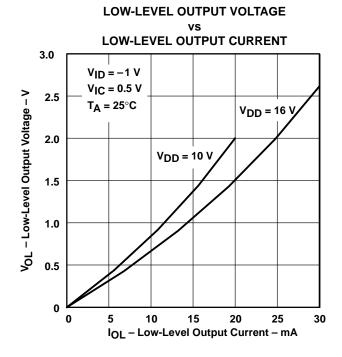


Figure 19

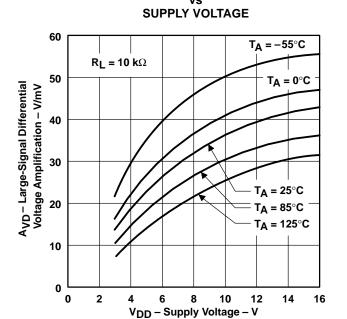


Figure 20

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

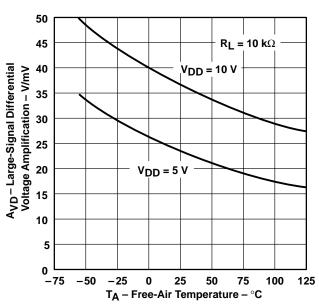


Figure 21

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



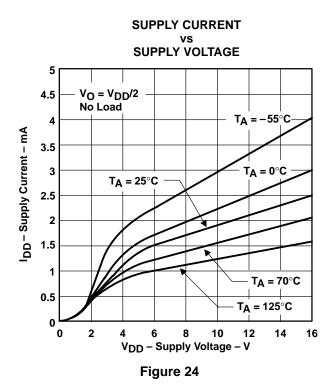
# INPUT BIAS CURRENT AND INPUT OFFSET CURRENT

# FREE-AIR TEMPERATURE 10000 IIB and IIO - Input Bias and Offset Currents - pA V<sub>DD</sub> = 10 V V<sub>IC</sub> = 5 V See Note A 1000 lιΒ 100 llo 10 1 0.1 <del>-</del> 25 65 75 85 95 105

NOTE A: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

## Figure 22

T<sub>A</sub> - Free-Air Temperature - °C



# COMMON-MODE INPUT VOLTAGE POSITIVE LIMIT VS SUPPLY VOLTAGE

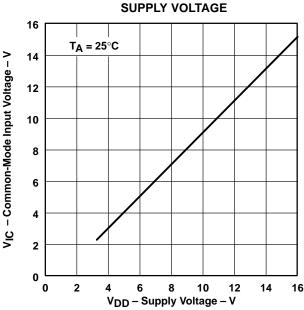


Figure 23

# SUPPLY CURRENT vs

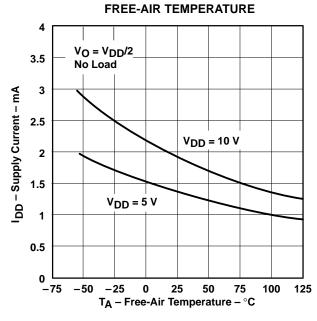


Figure 25

<sup>†</sup> Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



**SLEW RATE** 

vs

### TYPICAL CHARACTERISTICS<sup>†</sup>

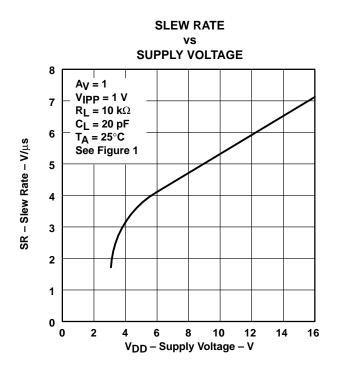


Figure 26

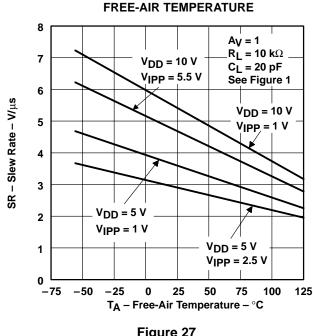
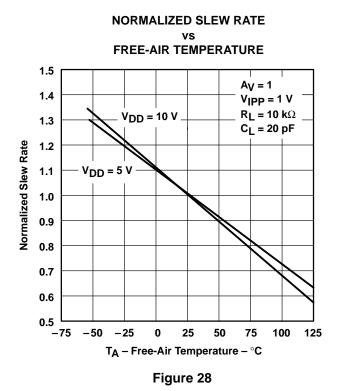
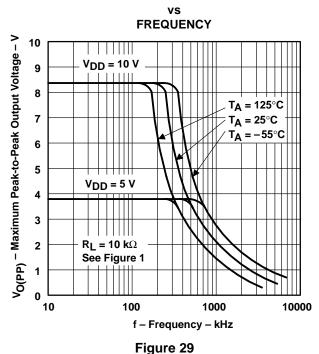


Figure 27

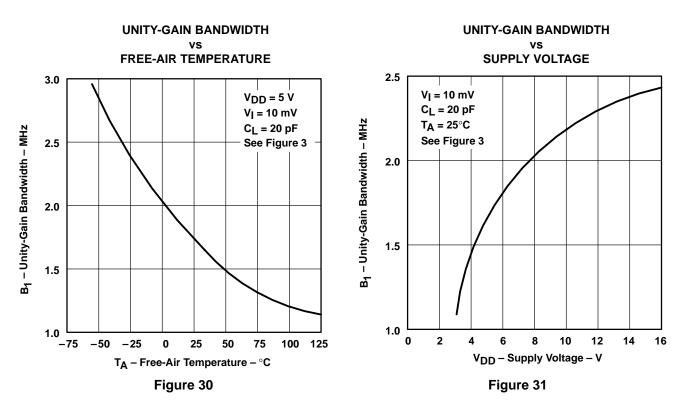


## **MAXIMUM PEAK OUTPUT VOLTAGE**



† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.





# LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT

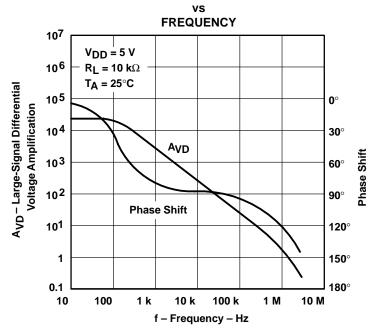


Figure 32

<sup>†</sup> Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



# LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT

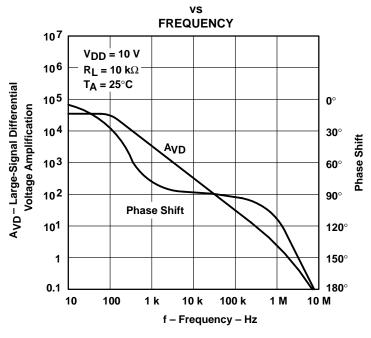
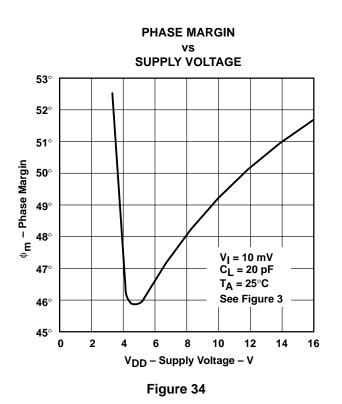
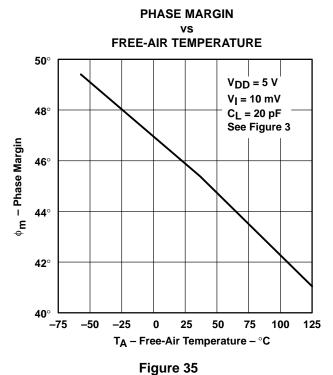


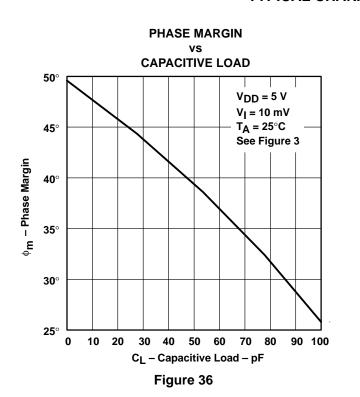
Figure 33

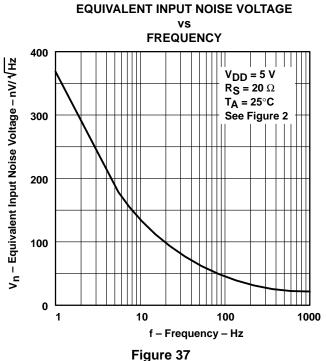




† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

## TYPICAL CHARACTERISTICS





### single-supply operation

While the TLC272 and TLC277 perform well using dual power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This design includes an input common-mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 3 V (C-suffix types), thus allowing operation with supply levels commonly available for TTL and HCMOS; however, for maximum dynamic range, 16-V single-supply operation is recommended.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. A resistive voltage divider is usually sufficient to establish this reference level (see Figure 38). The low input bias current of the TLC272 and TLC277 permits the use of very large resistive values to implement the voltage divider, thus minimizing power consumption.

The TLC272 and TLC277 work well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

- 1. Power the linear devices from separate bypassed supply lines (see Figure 39); otherwise, the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
- 2. Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, high-frequency applications may require RC decoupling.

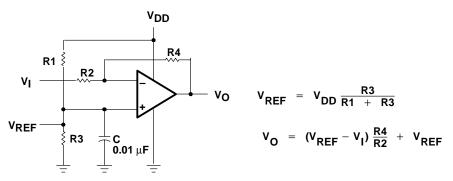
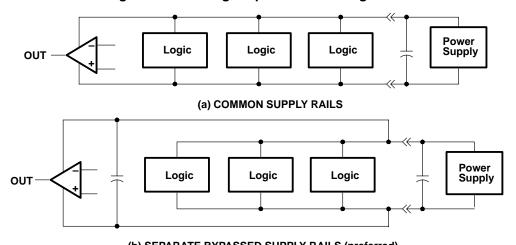


Figure 38. Inverting Amplifier With Voltage Reference



(b) SEPARATE BYPASSED SUPPLY RAILS (preferred)

Figure 39. Common vs Separate Supply Rails



### input characteristics

The TLC272 and TLC277 are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. Note that the lower range limit includes the negative rail, while the upper range limit is specified at  $V_{DD}-1$  V at  $T_A=25^{\circ}$ C and at  $V_{DD}-1.5$  V at all other temperatures.

The use of the polysilicon-gate process and the careful input circuit design gives the TLC272 and TLC277 very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1  $\mu$ V/month, including the first month of operation.

Because of the extremely high input impedance and resulting low bias current requirements, the TLC272 and TLC277 are well suited for low-level signal processing; however, leakage currents on printed-circuit boards and sockets can easily exceed bias current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 4 in the Parameter Measurement Information section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 40).

Unused amplifiers should be connected as grounded unity-gain followers to avoid possible oscillation.

### noise performance

The noise specifications in operational amplifier circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TLC272 and TLC277 result in a very low noise current, which is insignificant in most applications. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50 k $\Omega$ , since bipolar devices exhibit greater noise currents.

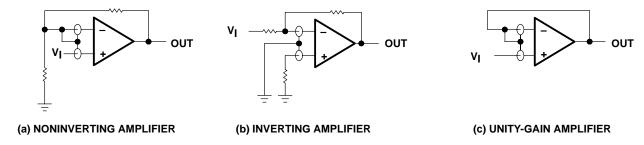


Figure 40. Guard-Ring Schemes

### output characteristics

The output stage of the TLC272 and TLC277 is designed to sink and source relatively high amounts of current (see typical characteristics). If the output is subjected to a short-circuit condition, this high current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

All operating characteristics of the TLC272 and TLC277 are measured using a 20-pF load. The devices can drive higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation (see Figure 41). In many cases, adding a small amount of resistance in series with the load capacitance alleviates the problem.



(d) TEST CIRCUIT

#### **APPLICATION INFORMATION**

## output characteristics (continued)

(c)  $C_L = 150 \text{ pF}$ ,  $R_L = NO \text{ LOAD}$ 

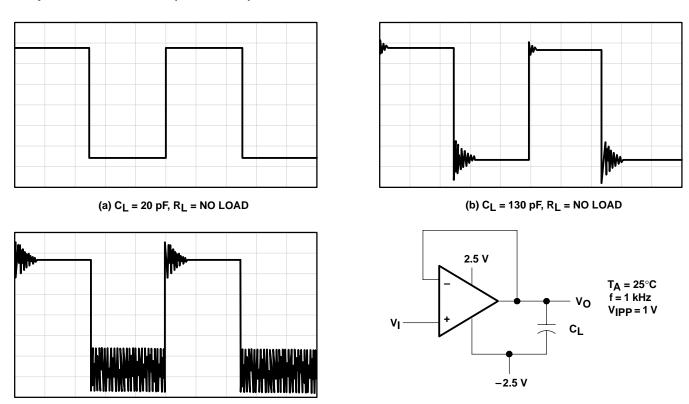
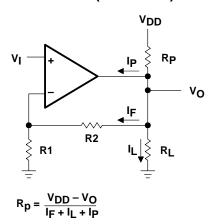


Figure 41. Effect of Capacitive Loads and Test Circuit

Although the TLC272 and TLC277 possess excellent high-level output voltage and current capability, methods for boosting this capability are available, if needed. The simplest method involves the use of a pullup resistor (Rp) connected from the output to the positive supply rail (see Figure 42). There are two disadvantages to the use of this circuit. First, the NMOS pulldown transistor N4 (see equivalent schematic) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on resistance between approximately 60  $\Omega$  and 180  $\Omega$ , depending on how hard the operational amplifier input is driven. With very low values of Rp, a voltage offset from 0 V at the output occurs. Second, pullup resistor Rp acts as a drain load to N4 and the gain of the operational amplifier is reduced at output voltage levels where N5 is not supplying the output current.

### output characteristics (continued)



 $I_p$  = Pullup current required by the operational amplifier (typically 500  $\mu$ A)

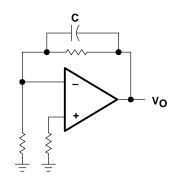


Figure 42. Resistive Pullup to Increase V<sub>OH</sub>

Figure 43. Compensation for Input Capacitance

#### feedback

Operational amplifier circuits almost always employ feedback, and since feedback is the first prerequisite for oscillation, some caution is appropriate. Most oscillation problems result from driving capacitive loads (discussed previously) and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 43). The value of this capacitor is optimized empirically.

### electrostatic discharge protection

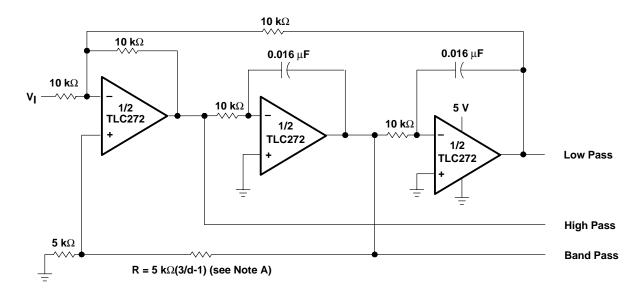
The TLC272 and TLC277 incorporate an internal electrostatic discharge (ESD) protection circuit that prevents functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised, however, when handling these devices as exposure to ESD may result in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse-biased diode.

#### latch-up

Because CMOS devices are susceptible to latch-up due to their inherent parasitic thyristors, the TLC272 and TLC277 inputs and outputs were designed to withstand -100-mA surge currents without sustaining latch-up; however, techniques should be used to reduce the chance of latch-up whenever possible. Internal protection diodes should not, by design, be forward biased. Applied input and output voltage should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1  $\mu$ F typical) located across the supply rails as close to the device as possible.

The current path established if latch-up occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and/or voltages on either the output or inputs that exceed the supply voltage. Once latch-up occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latch-up occurring increases with increasing temperature and supply voltages.





NOTE A: d = damping factor, 1/Q

Figure 44. State-Variable Filter

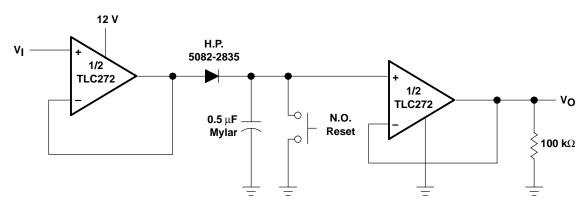
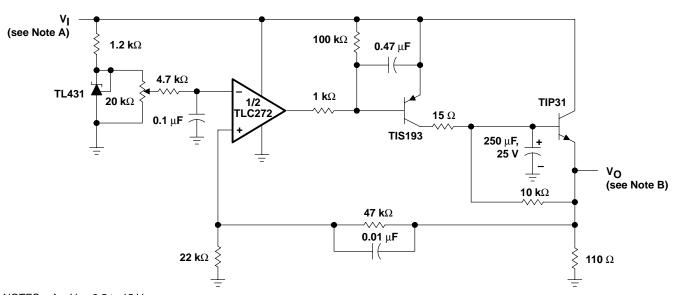
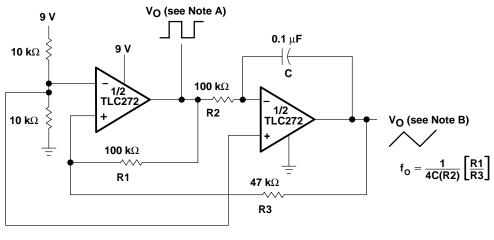


Figure 45. Positive-Peak Detector



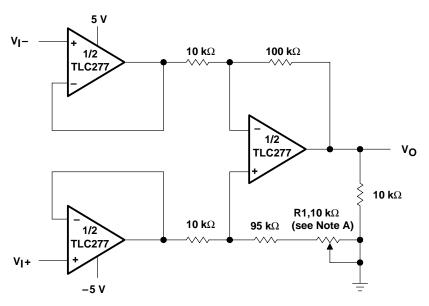
NOTES: A.  $V_I = 3.5$  to 15 V B.  $V_O = 2$  V, 0 to 1 A

Figure 46. Logic-Array Power Supply



NOTES: A.  $V_{O(PP)} = 8 \text{ V}$ B.  $V_{O(PP)} = 4 \text{ V}$ 

Figure 47. Single-Supply Function Generator



NOTE B: CMRR adjustment must be noninductive.

Figure 48. Low-Power Instrumentation Amplifier

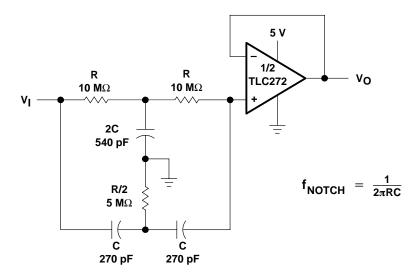


Figure 49. Single-Supply Twin-T Notch Filter





24-Jan-2013

## **PACKAGING INFORMATION**

Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Top-Side Markings	Sample
5962-89494022A	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI	-55 to 125	.,	
TLC272ACD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	272AC	Sample
TLC272ACDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	272AC	Sample
TLC272ACDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	272AC	Sample
TLC272ACDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	272AC	Sample
TLC272ACP	ACTIVE	PDIP	Р	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TLC272ACP	Sample
TLC272ACPE4	ACTIVE	PDIP	Р	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TLC272ACP	Sample
TLC272AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	272AI	Sample
TLC272AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	272AI	Sample
TLC272AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	272AI	Sample
TLC272AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	272AI	Sample
TLC272AIP	ACTIVE	PDIP	Р	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TLC272AIP	Sample
TLC272AIPE4	ACTIVE	PDIP	Р	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TLC272AIP	Sample
TLC272BCD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	272BC	Sample
TLC272BCDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	272BC	Sample
TLC272BCDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	272BC	Sample
TLC272BCDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	272BC	Sampl





www.ti.com

24-Jan-2013

Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Top-Side Markings	Samples
TLC272BCP	ACTIVE	PDIP	Р	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TLC272BCP	Samples
TLC272BCPE4	ACTIVE	PDIP	Р	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TLC272BCP	Samples
TLC272BID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	272BI	Samples
TLC272BIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	272BI	Samples
TLC272BIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	272BI	Samples
TLC272BIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	272BI	Samples
TLC272BIP	ACTIVE	PDIP	Р	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TLC272BIP	Samples
TLC272BIPE4	ACTIVE	PDIP	Р	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TLC272BIP	Samples
TLC272CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	272C	Samples
TLC272CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	272C	Samples
TLC272CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	272C	Samples
TLC272CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	272C	Samples
TLC272CP	ACTIVE	PDIP	Р	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TLC272CP	Samples
TLC272CPE4	ACTIVE	PDIP	Р	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TLC272CP	Samples
TLC272CPSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	P272	Samples
TLC272CPSRG4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	P272	Samples
TLC272CPW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	P272C	Samples
TLC272CPWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	P272C	Samples





www.ti.com 24-Jan-2013

Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead/Ball Finish		Op Temp (°C)		Samples
TLC272CPWLE	OBSOLETE	TSSOP	PW	8		(2) TBD	Call TI	(3) Call TI	0 to 70	(4)	
TLC272CPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	P272C	Sample
TLC272CPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	P272C	Sample
TLC272ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2721	Sample
TLC272IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2721	Sample
TLC272IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2721	Sample
TLC272IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2721	Sample
TLC272IP	ACTIVE	PDIP	Р	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TLC272IP	Sample
TLC272IPE4	ACTIVE	PDIP	Р	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TLC272IP	Sample
TLC272MFKB	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI	-55 to 125		
TLC272MJG	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI	-55 to 125		
TLC272MJGB	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI	-55 to 125		
TLC272P-M	PREVIEW	PDIP	Р	8		TBD	Call TI	Call TI			
TLC277CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		277C	Sample
TLC277CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		277C	Sample
TLC277CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		277C	Sample
TLC277CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		277C	Sample
TLC277CP	ACTIVE	PDIP	Р	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type		TLC277CP	Sample
TLC277CPE4	ACTIVE	PDIP	Р	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type		TLC277CP	Sample
TLC277CPSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		P277	Sample





www.ti.com 24-Jan-2013

Orderable Device	Status	Package Type	•	Pins	Package Qty	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Top-Side Markings	Samples
	(1)		Drawing			(2)		(3)		(4)	
TLC277CPSRG4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		P277	Samples
TLC277ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2771	Samples
TLC277IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2771	Samples
TLC277IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2771	Samples
TLC277IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2771	Samples
TLC277IP	ACTIVE	PDIP	Р	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type		TLC277IP	Samples
TLC277IPE4	ACTIVE	PDIP	Р	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type		TLC277IP	Samples
TLC277MFKB	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI	-55 to 125		
TLC277MJG	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI	-55 to 125		
TLC277MJGB	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI	-55 to 125		

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.



### **PACKAGE OPTION ADDENDUM**

24-Jan-2013

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

<sup>(4)</sup> Only one of markings shown within the brackets will appear on the physical device.

PACKAGE MATERIALS INFORMATION

www.ti.com 26-Jan-2013

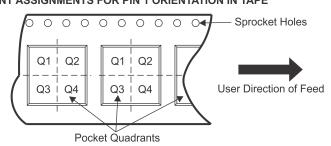
### TAPE AND REEL INFORMATION



# TAPE DIMENSIONS KO P1 BO W Cavity A0

	Dimension designed to accommodate the component width
	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

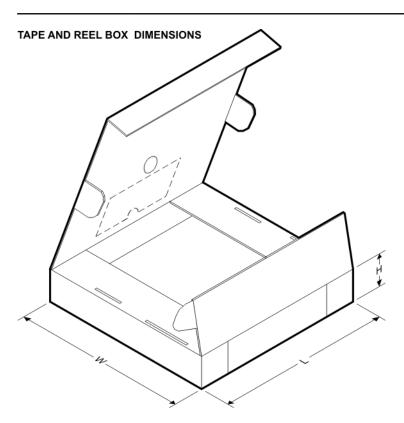
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



### \*All dimensions are nominal

*All dimensions are nominal				1								
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC272ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC272AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC272BCDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC272BIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC272CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC272CPSR	SO	PS	8	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
TLC272CPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLC272IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC277CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC277CPSR	SO	PS	8	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
TLC277IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

www.ti.com 26-Jan-2013



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC272ACDR	SOIC	D	8	2500	340.5	338.1	20.6
TLC272AIDR	SOIC	D	8	2500	340.5	338.1	20.6
TLC272BCDR	SOIC	D	8	2500	340.5	338.1	20.6
TLC272BIDR	SOIC	D	8	2500	340.5	338.1	20.6
TLC272CDR	SOIC	D	8	2500	340.5	338.1	20.6
TLC272CPSR	SO	PS	8	2000	367.0	367.0	38.0
TLC272CPWR	TSSOP	PW	8	2000	367.0	367.0	35.0
TLC272IDR	SOIC	D	8	2500	340.5	338.1	20.6
TLC277CDR	SOIC	D	8	2500	340.5	338.1	20.6
TLC277CPSR	SO	PS	8	2000	367.0	367.0	38.0
TLC277IDR	SOIC	D	8	2500	340.5	338.1	20.6

### JG (R-GDIP-T8)

### **CERAMIC DUAL-IN-LINE**



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification.
- E. Falls within MIL STD 1835 GDIP1-T8

# FK (S-CQCC-N\*\*)

# LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004



# P (R-PDIP-T8)

# PLASTIC DUAL-IN-LINE PACKAGE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS-001 variation BA.



# D (R-PDSO-G8)

### PLASTIC SMALL OUTLINE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.



# D (R-PDSO-G8)

# PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.





NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



# PS (R-PDSO-G8)

# PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



PW (R-PDSO-G8)

# PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153



### IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have *not* been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

### Products Applications

Audio www.ti.com/audio Automotive and Transportation www.ti.com/automotive Communications and Telecom **Amplifiers** amplifier.ti.com www.ti.com/communications **Data Converters** dataconverter.ti.com Computers and Peripherals www.ti.com/computers **DLP® Products** www.dlp.com Consumer Electronics www.ti.com/consumer-apps

DSP **Energy and Lighting** dsp.ti.com www.ti.com/energy Clocks and Timers www.ti.com/clocks Industrial www.ti.com/industrial Interface interface.ti.com Medical www.ti.com/medical logic.ti.com Logic Security www.ti.com/security

Power Mgmt power.ti.com Space, Avionics and Defense www.ti.com/space-avionics-defense

Microcontrollers microcontroller.ti.com Video and Imaging www.ti.com/video

RFID www.ti-rfid.com

OMAP Applications Processors <a href="www.ti.com/omap">www.ti.com/omap</a> TI E2E Community <a href="e2e.ti.com">e2e.ti.com</a>

Wireless Connectivity <u>www.ti.com/wirelessconnectivity</u>